ABSTRACT OF THE DISCLOSURE

A method and apparatus for reducing instruction ITLB accesses. In one embodiment, the method may comprise generating a next virtual fetch address corresponding to an instruction fetch request and determining whether a current physical address translation is valid for the next virtual fetch address in response to its generation, wherein the determination may comprise detecting a change in the virtual page number of the next virtual fetch address relative to a virtual page number of a current virtual fetch address. The method may further comprise activating an ITLB circuit in response to determining that the current physical address translation is not valid for the next virtual fetch address, and performing the instruction fetch using the current physical address translation without activating the ITLB circuit in response to determining that the current physical address translation is valid for said next virtual fetch address.